IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently Amended): An audio processor which processes an input data stream via an external memory, comprising:

a control processor to fetch in, when executing one of divided procedures of an audio process, a program and audio data corresponding to a next one of the procedures from the external memory which stores programs and a group of data used for sequentially executing the divided procedures of the audio process;

an internal memory to store the program and audio data fetched from the external memory by the control processor and corresponding to the one and the next one of the procedures, the internal memory including an instruction memory configured to store an instruction group of the program transferred from the external memory and a data memory configured to store a data group transferred from the external memory;

a coprocessor to subserve the control processor to subject audio data of the input data stream to the divided procedures of the audio process sequentially, based on the program fetched by the control processor, the coprocessor executing multiplication/accumulation addition according to VLIW (Very Long Instruction Word)[[,]]; and

a DMA controller to control writing of data to the external memory, writing of the instruction group to the instruction memory, and writing of the data group to the data memory, and reading of the data and the data group from the external memory and the data memory by DMA (Direct Memory Access) transfer,

wherein ~~the internal memory comprises an instruction memory configured to store an instruction group of the program transferred from the external memory and a data memory configured to store a data group transferred from the external memory, and~~ the coprocessor subserves the control processor to perform the process based on the instruction group using the data in the data memory and data corresponding to a progress stage of audio data reconstruction to generate audio data, and

wherein the control processor makes reservation of sending an instruction to the DMA controller so that the data and instruction group required for the next processing is prepared in advance while continuing the processing which is currently performed~~ a space required in the instruction memory and the data memory of the internal memory for the instructions and the data of the audio process for the next one of the procedures is reserved by the control processor, thereby configured to allow preparation of the data and the instructions in the internal memory before the next one of the procedures starts~~.

Claim 2 (Previously Presented): An audio processor according to claim 1, wherein the coprocessor is configured to subserve the control processor to subject sequentially the audio data to decoding, noise-less decoding, noise reduction, filter bank, and block switching in accordance with the programs and data fetched from the external memory in units of one procedure.

Claim 3 (Previously Presented): An audio processor according to claim 2, wherein the coprocessor is configured to subserve the control processor to execute the program fetched in the internal memory from the external memory in accordance with progress of the procedures of the audio process.

Claims 4-7 (Previously Cancelled).

Claim 8 (Previously Presented): An audio processor according to claim 1, wherein the control processor sequentially transfers a plurality of program modules corresponding to procedures of the audio process to the coprocessor from the external memory according to the progress of the procedures.

Claim 9 (Previously Presented): An audio processor according to claim 1, wherein the coprocessor subserves the control processor to execute decoding of bit stream data, noiseless decoding, inverse quantization, scale factor, TNS processing, filter bank processing, and the block switching, in this order, to reconstruct audio data.

Claim 10 (Previously Presented): An audio processor according to claim 9, wherein the control processor includes a function of predicting which procedure is performed after the procedure which is currently performed.

Claim 11-13 (Previously Cancelled).

Claim 14 (Previously Presented): An audio processor according to claim I wherein the control processor is further configured to release a storage region of the internal memory occupied by the data stored in the internal memory or a program if the data stored in the internal memory or the program becomes unused by the coprocessor.

Claims 15-23 (Previously Cancelled).

Claim 24 (Previously Presented): The audio processor according to claim 1, wherein the internal memory includes an instruction memory and a data memory, and at least two parallel busses lead from the instruction memory and the data memory to the coprocessor.

Claims 25-29 (Previously Cancelled).

Claim 30 (Previously Presented): The audio processor according to claim 1, further comprising:

an audio input/output interface; and

an internal bus;

wherein the internal bus links the control processor, the coprocessor and the audio input/output interface together.

Claim 31 (Previously Canceled).

Claims 32-33 (Cancelled).

Claim 34 (Previously Presented): The audio processor according to Claim 1, wherein the divided procedures of the audio process include five different processing stages performed sequentially, the five different processing stages using different memory spaces of the data memory in the internal memory.